P-Channel Enhancement Mode Field Effect Transistor

Features

$V_{DS\ (V)}$ = -30V，I_D = -5A，

$R_{DS(ON)}$＜43mR @V_{GS} = -10V

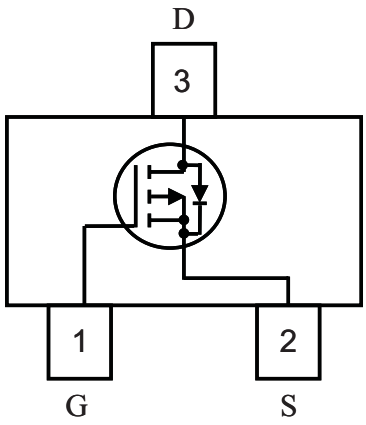
Voltage controlled p-channel small signal switch

High density cell design for low $R_{DS(ON)}$

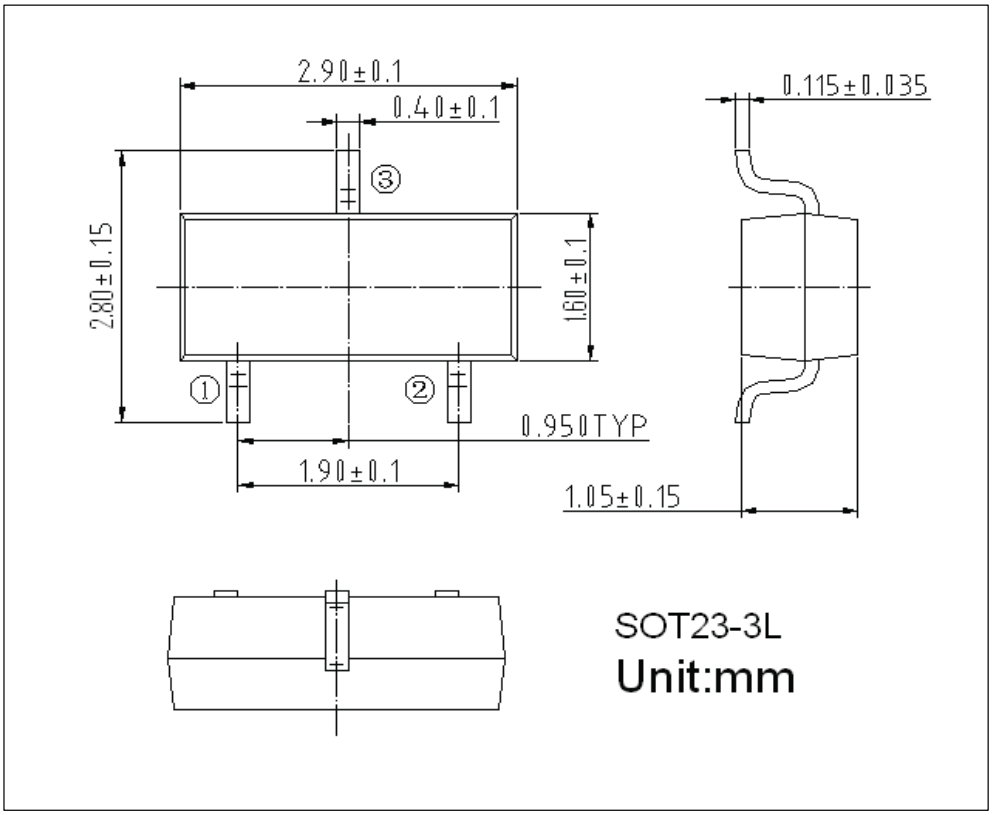
General Description

This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package Excellent thermal and electrical capabilities.

Pin Configurations



Package Information



- **Absolute Maximum Ratings** @T_A=25℃ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±12	V
Maximum Drain Current	DC and TA=25℃	I_{D25}	-5.0	A
	DC and TA=70℃	I_{D70}	-4.0	
	Pulsed	I_{DM}	-30	
Continuous Power Dissipation		P_D	1.4	W
Operating and Storage Temperature Range		T_J,T_{STG}	-55 to 150	℃

- **Electrical Characteristics** @T_A=25℃ unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} =0V	--	--	-1	μA
Gate - Body Leakage, Forward	I_{GSSF}	V_{GS} = -12V	--	--	-100	nA
Gate - Body Leakage, Reverse	I_{GSSR}	V_{GS} = 12V	--	--	100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS\ (TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.7	-1.0	-1.3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -5A	--	--	43	mR
		V_{GS} = -4.5V, I_D = -4A	--	--	55	
		V_{GS} = -2.5V, I_D = -1A	--	--	110	
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS} = -30V, V_{GS} = 0V, F = 200KHz	--	600	--	pF
Output Capacitance	C_{OSS}		--	85	--	pF
Reverse Transfer Capacitance	C_{RSS}		--	566	--	pF
SWITCHING CHARACTERISTICS						
Turn-on Delay Time	$T_{D\ (ON)}$	V_{GS}=-10V, V_{DS}=-15V, R_L=3.6R,R_{GEN}=6R	--	6.5	--	ns
Rise Time	T_R		--	3.5	--	
Turn-off Delay Time	$T_{D(OFF)}$		--	40	--	
Fall Time	T_F		--	13	--	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Body Diode Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = -1A	--	-0.78	-1	V

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

- **Typical Performance Characteristics**

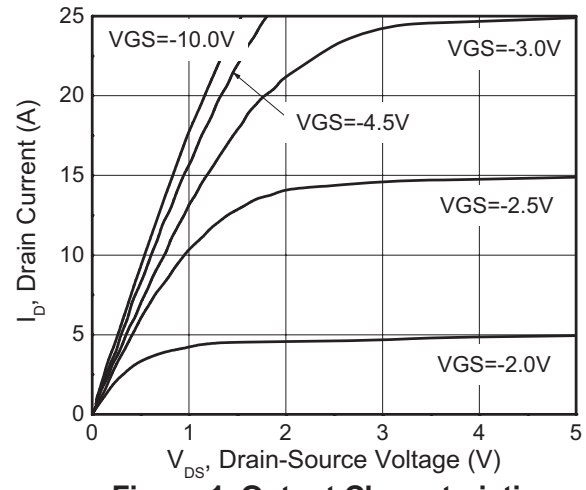


Figure 1. Output Characteristics

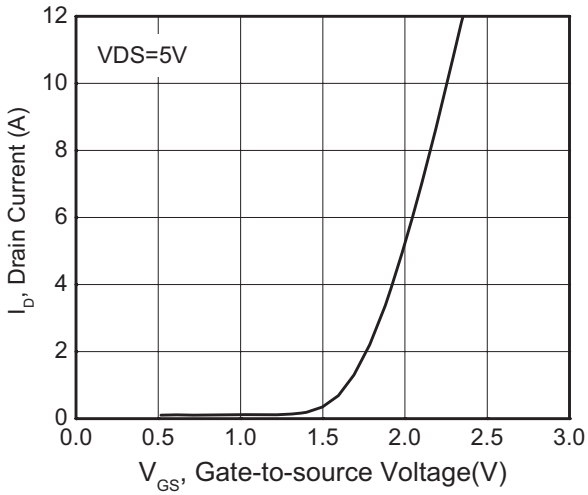


Figure 2. Transfer Characteristics

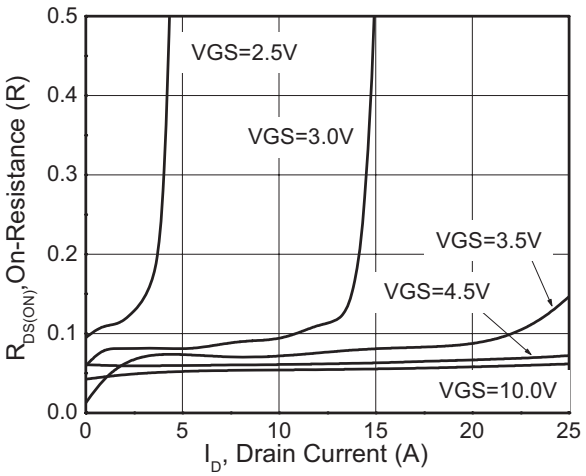


Figure 3. On Resistance VS I_d

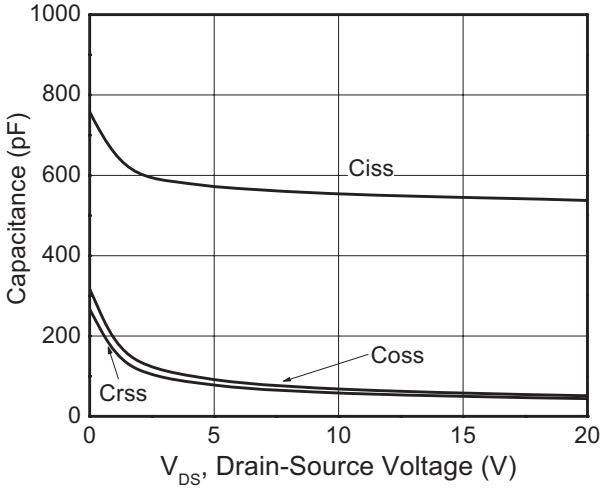


Figure 4. Capacitance

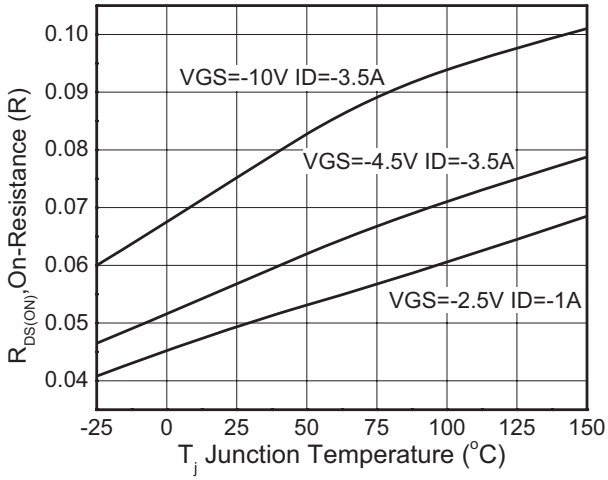


Figure 5 . On-resistance VS Temperature

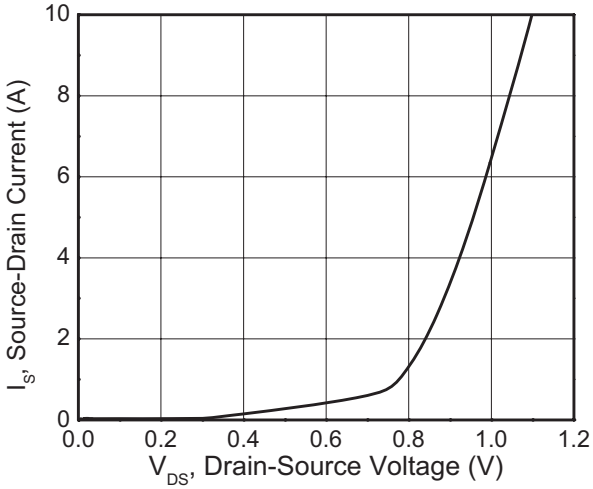


Figure 6. Body Diode Characteristics

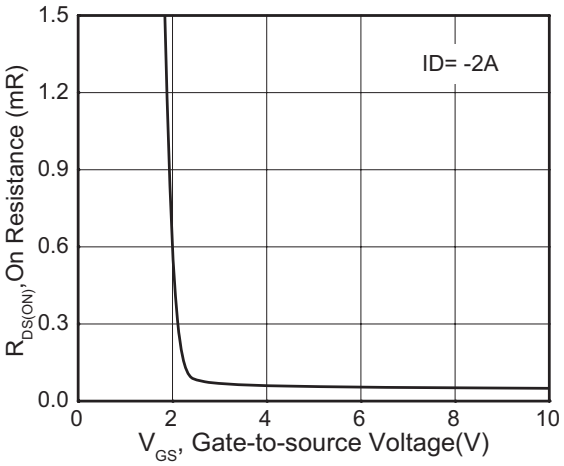


Figure 7. On Resistance VS V_{GS}

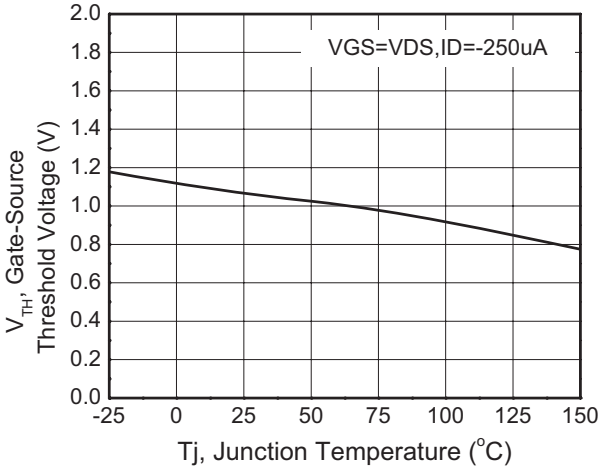


Figure 8. Gate Threshold Vs. Temperature

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