



## P-Channel Enhancement Mode Field Effect Transistor

- Features**

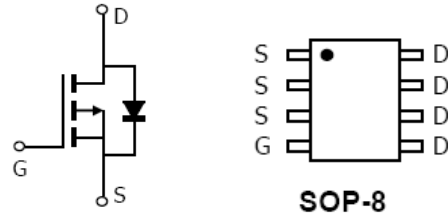
$V_{DS} (V) = -40V$

$I_D = -6 A (V_{GS} = -10V)$

$R_{DS(ON)} < 40m\Omega (V_{GS} = -10V)$

$R_{DS(ON)} < 80m\Omega (V_{GS} = -4.5V)$

- Pin Configurations**



- General Description**

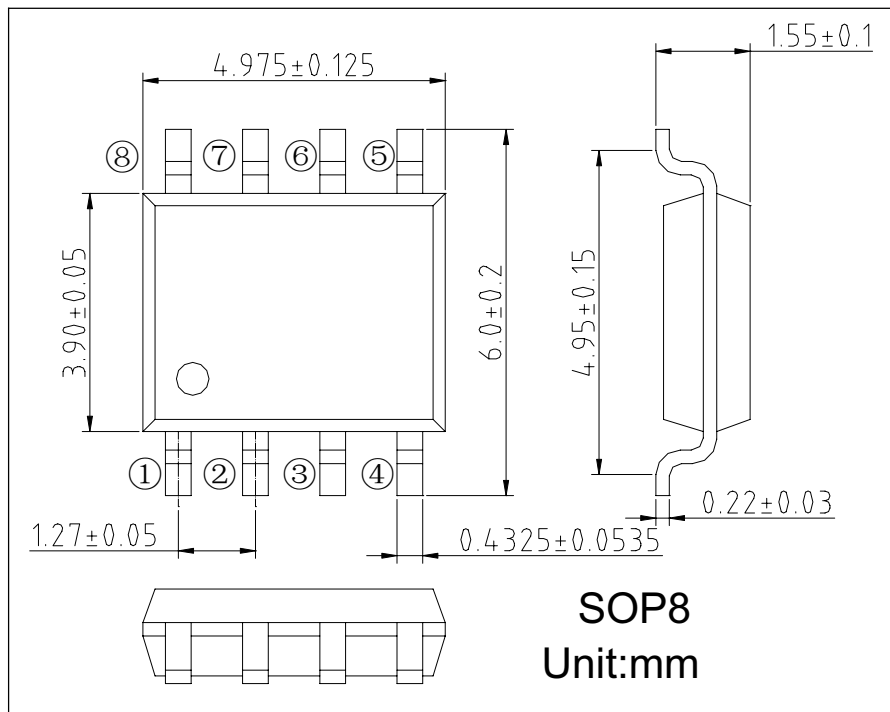
The HX4443SQ/L uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , and ultra-low low gate charge.

This device is suitable for use as a load switch or in PWM applications. HX4443SQ and HX4443SQL are electrically identical.

-RoHS Compliant

-HX4443SQL is Halogen Free

- Package Information**



- Absolute Maximum Ratings @ $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DSS}$	-40	V



# HX4443SQ

Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Drain Current (Continuous) *AC	$T_A=25^\circ\text{C}$	$I_D$	-6	A
	$T_A=70^\circ\text{C}$		-4.8	
Drain Current (Pulse) *B		$I_{DM}$	-18	A
Power Dissipation	$T_A=25^\circ\text{C}$	$P_D$	3	W
	$T_A=70^\circ\text{C}$		2.1	
Operating Temperature/ Storage Temperature		$T_{J}/T_{STG}$	-55~150	$^\circ\text{C}$

## ● Electrical Characteristics @ $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -32V, V_{GS} = 0V$	--	--	-1	$\mu A$
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_{DS} = -250\mu A$	-1.0	-2	-2.5	V
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$	--	--	100	nA
Drain-Source On-state Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -5.5A$	--	33	40	m $\Omega$
		$V_{GS} = -4.5V, I_D = -4.5A$	--	64	80	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{GS} = -10V, I_D = -5.5A$	--	11	--	S
Diode Forward Voltage	$V_{SD}$	$I_{SD} = -1A, V_{GS} = 0V$	--	-0.75	-1.0	V
Maximum Body-Diode Continuous Current	$I_S$		--	--	-5	A
<b>Switching</b>						
Total Gate Charge	$Q_g$	$V_{GS} = -10V, V_{DS} = -20V,$ $I_D = -5.5A$	--	14	--	nC
Gate-Source Charge	$Q_{gs}$		--	2.2	--	nC
Gate-Drain Charge	$Q_{gd}$		--	1.9	--	nC
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DS} = -20V,$ $R_L = 3.7\Omega, R_{GEN} = 3\Omega$	--	7.7	15.4	ns
Turn-on Rise Time	$t_r$		--	8	16	ns
Turn-off Delay Time	$t_{d(off)}$		--	26.5	53	ns
Turn-off Fall Time	$t_f$		--	11.5	23	ns
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -20V,$ $f = 1MHz$	--	690	--	pF
Output Capacitance	$C_{oss}$		--	310	--	pF
Reverse Transfer Capacitance	$C_{rss}$		--	75	--	pF

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The current rating is based on the  $t \leq 10s$  junction to ambient thermal resistance rating.



● TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

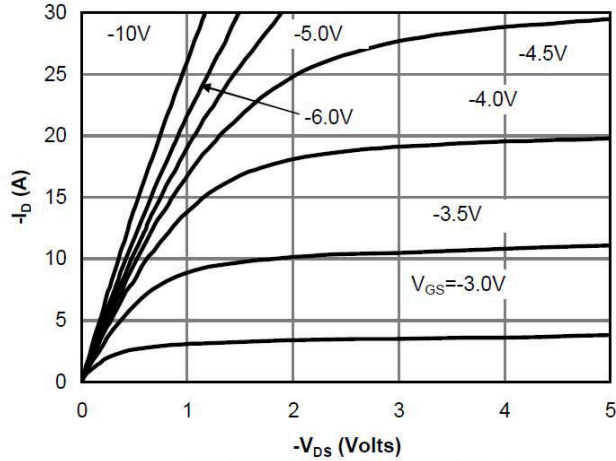


Fig 1: On-Region Characteristics

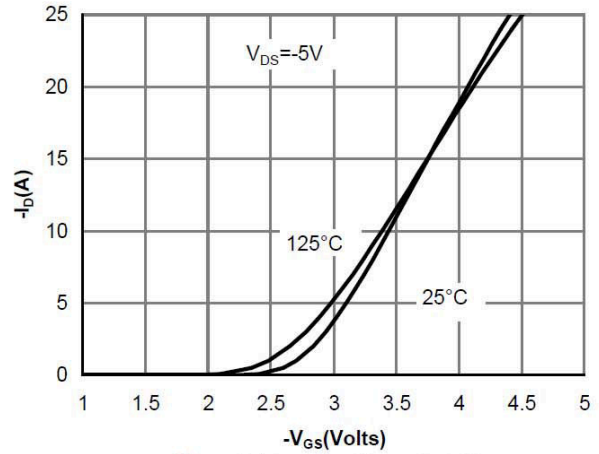


Figure 2: Transfer Characteristics

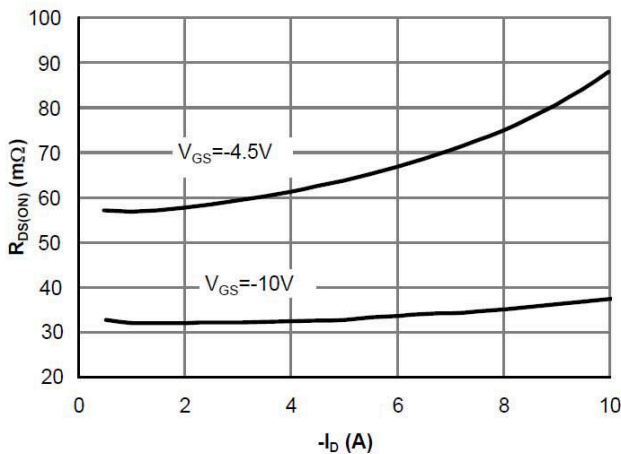


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

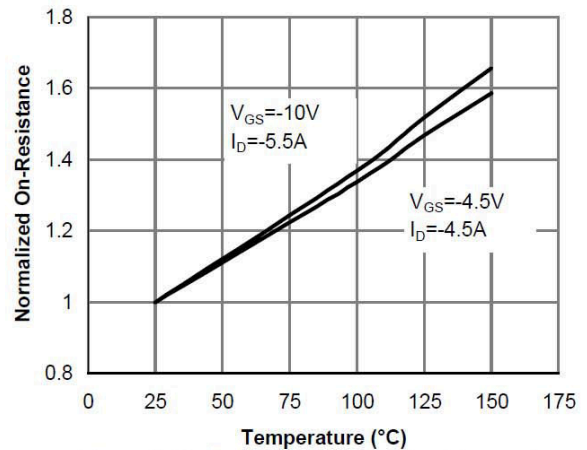


Figure 4: On-Resistance vs. Junction Temperature

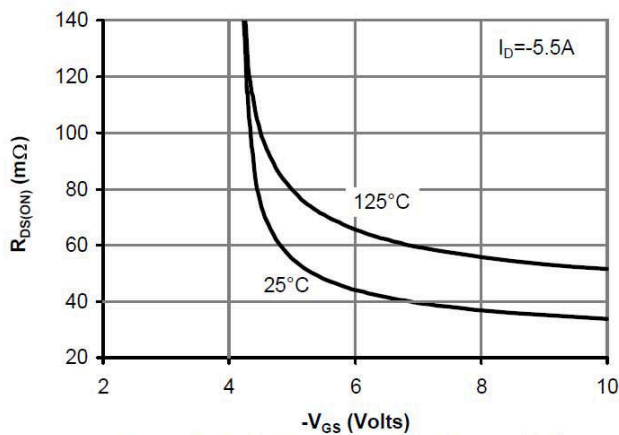


Figure 5: On-Resistance vs. Gate-Source Voltage

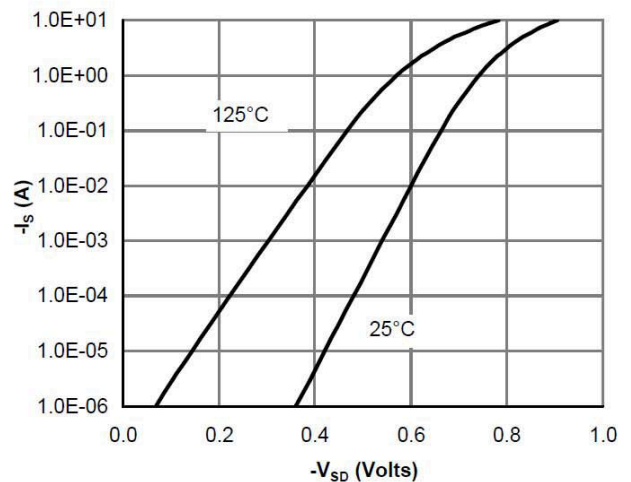


Figure 6: Body-Diode Characteristics

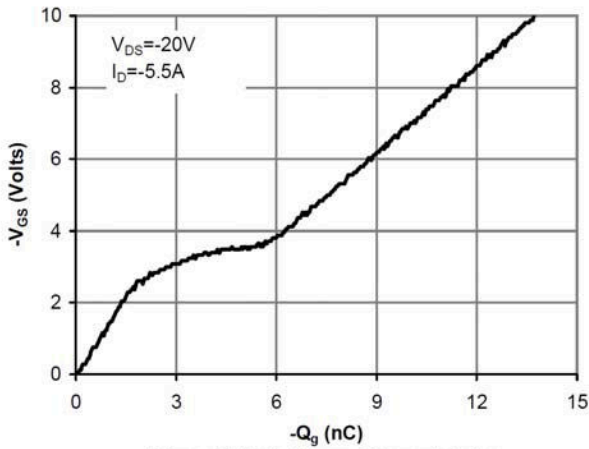


Figure 7: Gate-Charge Characteristics

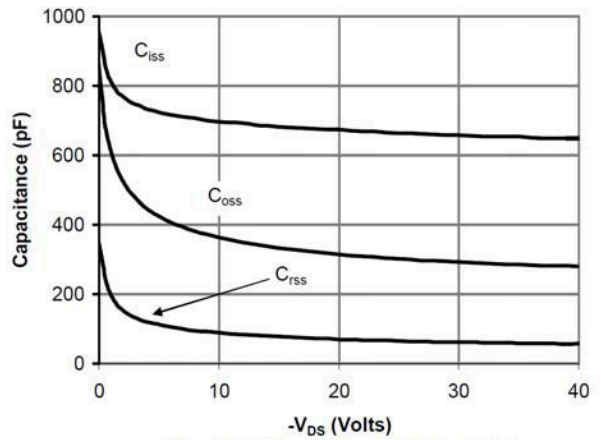


Figure 8: Capacitance Characteristics

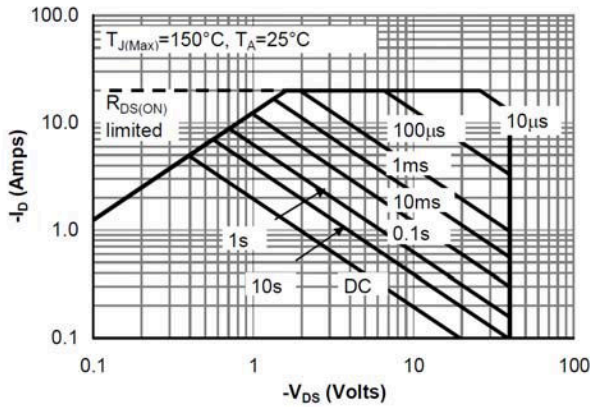


Figure 9: Maximum Forward Biased Safe Operating Area

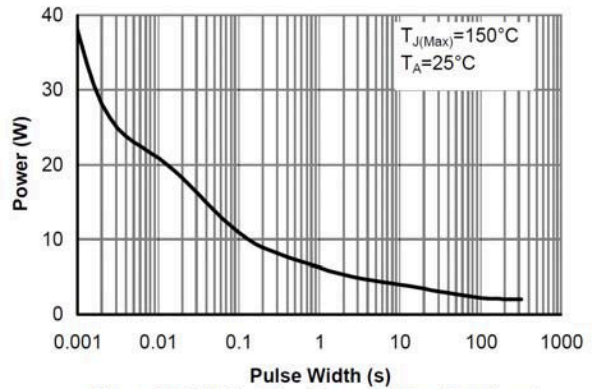


Figure 10: Single Pulse Power Rating Junction-to-Ambient

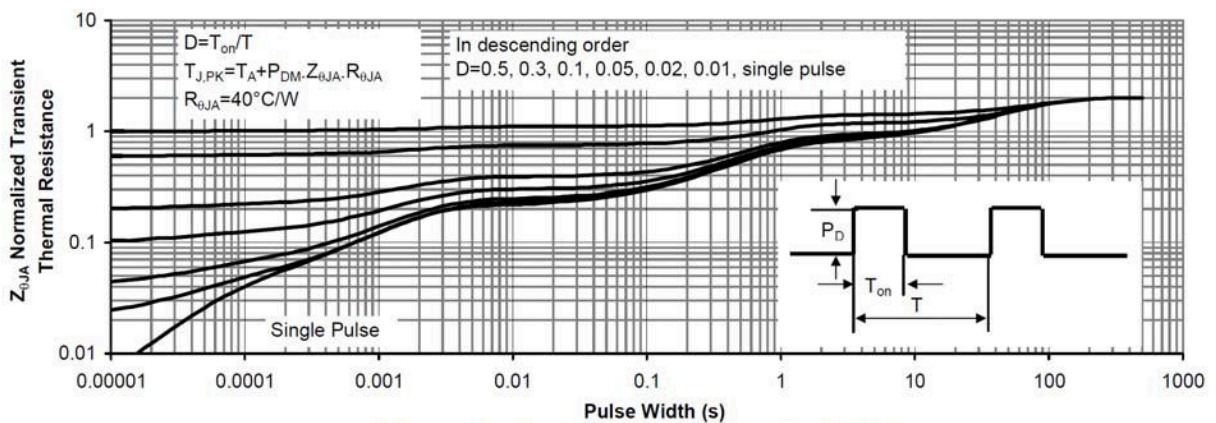


Figure 11: Normalized Maximum Transient Thermal Impedance



**DISCLAIMER**

HUAXIN SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. HUAXIN DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENCE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.