



N-Channel Enhancement Mode Field Effect Transistor

● Features

$V_{DS} (V) = 40V$

$I_D = 8A (V_{GS} = 10V)$

$R_{DS(ON)} < 30m\Omega (V_{GS} = 10V)$

$R_{DS(ON)} < 40m\Omega (V_{GS} = 4.5V)$

● General Description

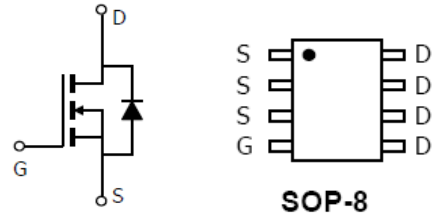
The HX4445SQ/L uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. The source leads are separated to allow a Kelvin connection to the source, which may be used to bypass the source inductance.

HX4445SQ and HX4445SQL are electrically identical.

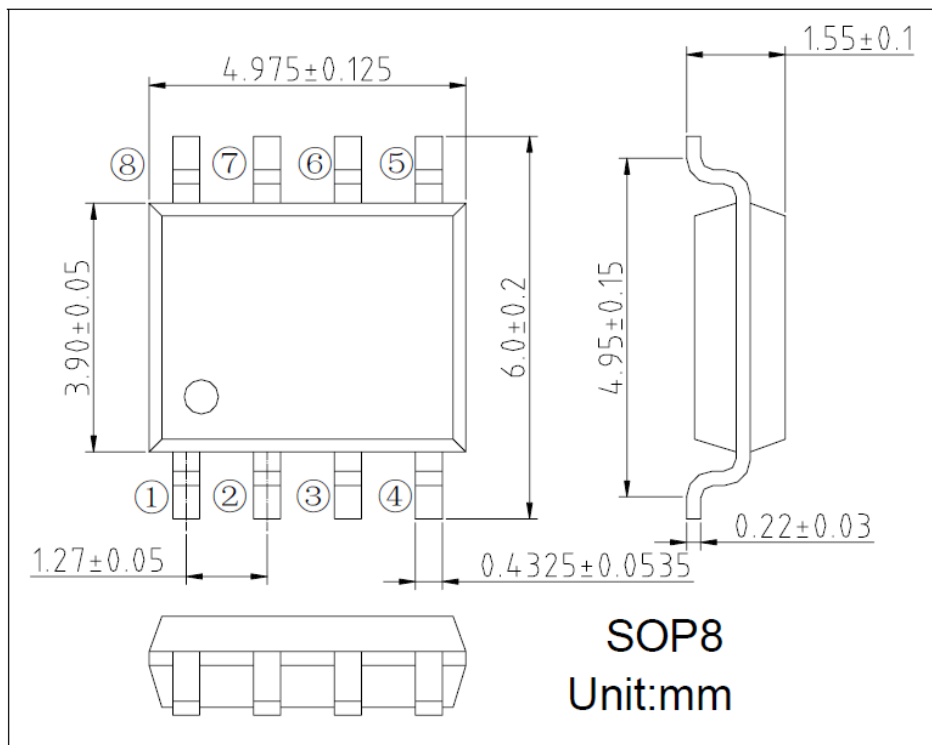
-RoHS Compliant

-HX4445SQL is Halogen Free

● Pin Configurations



● Package Information





● **Absolute Maximum Ratings @ $T_A=25^{\circ}\text{C}$ unless otherwise noted**

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DSS}	40	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current (Continuous) *AC	I_D	$T_A=25^{\circ}\text{C}$	8
		$T_A=70^{\circ}\text{C}$	6
Drain Current (Pulse) *B	I_{DM}	30	A
Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	2.5
		$T_A=70^{\circ}\text{C}$	2
Operating Temperature/ Storage Temperature	T_{J}/T_{STG}	-55~150	$^{\circ}\text{C}$

● **Electrical Characteristics @ $T_A=25^{\circ}\text{C}$ unless otherwise noted**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$	--	--	1	μA
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_{DS} = 250\mu\text{A}$	1	1.8	3	V
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	--	--	100	nA
Drain-Source On-state Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 8A$	--	21	30	m Ω
		$V_{GS} = 4.5V, I_D = 6A$	--	29	40	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5V, I_D = 8A$	--	16	--	S
Diode Forward Voltage	V_{SD}	$I_{SD} = 1A, V_{GS} = 0V$	--	0.7	1.1	V
Maximum Body-Diode Continuous Current	I_S		--	--	4.3	A
Switching						
Total Gate Charge	Q_g	$V_{GS} = 10V, V_{DS} = 20V, I_D = 8A$	--	14.68	--	nC
Gate-Source Charge	Q_{gs}		--	2.16	--	nC
Gate-Drain Charge	Q_{gd}		--	2.47	--	nC
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DS} = 20V, R_L = 2.5\Omega, R_{GEN} = 3\Omega$	--	9.55	--	ns
Turn-on Rise Time	t_r		--	3.22	--	ns
Turn-off Delay Time	$t_{d(off)}$		--	26.14	--	ns
Turn-off Fall Time	t_f		--	2.73	--	ns
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 20V, f = 1\text{MHz}$	--	799.16	--	pF
Output Capacitance	C_{oss}		--	105.93	--	pF
Reverse Transfer Capacitance	C_{riss}		--	67.61	--	pF

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The current rating is based on the $t \leq 10\text{s}$ junction to ambient thermal resistance rating.



● TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

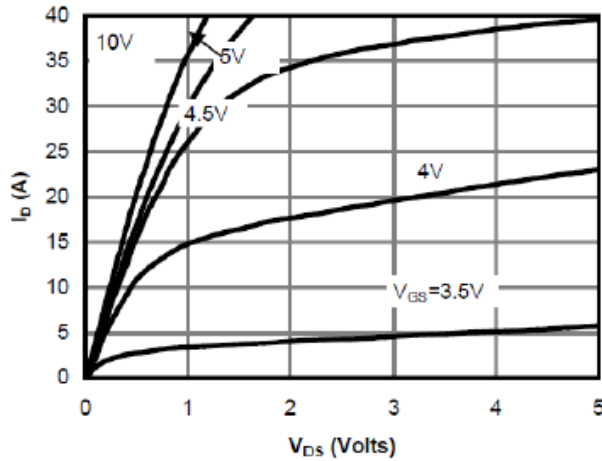


Fig 1: On-Region Characteristics

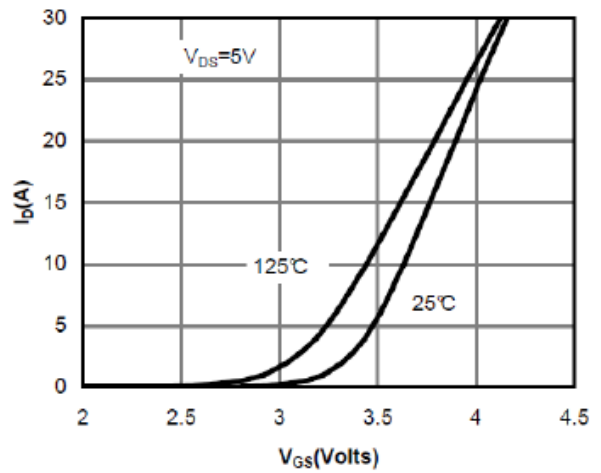


Figure 2: Transfer Characteristics

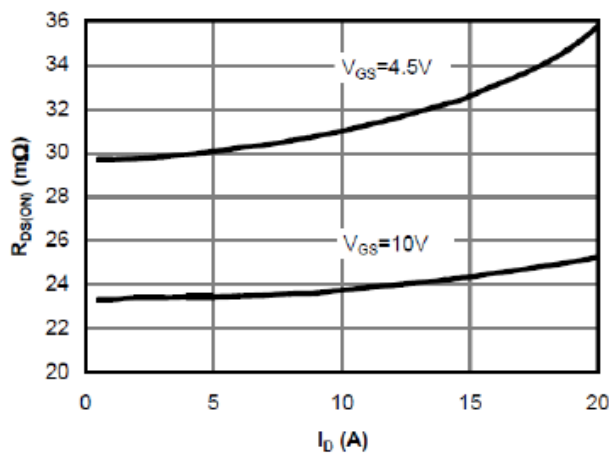


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

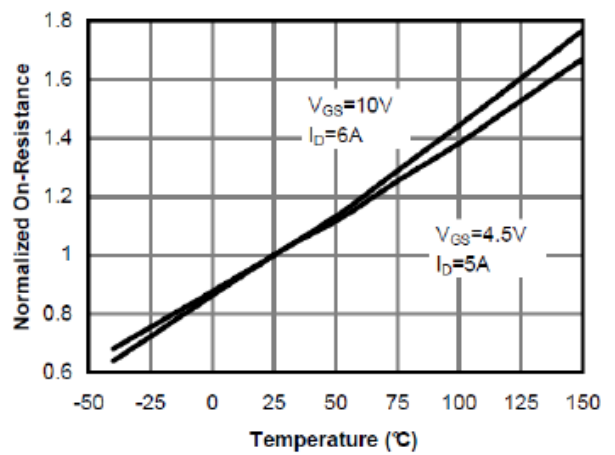


Figure 4: On-Resistance vs. Junction Temperature

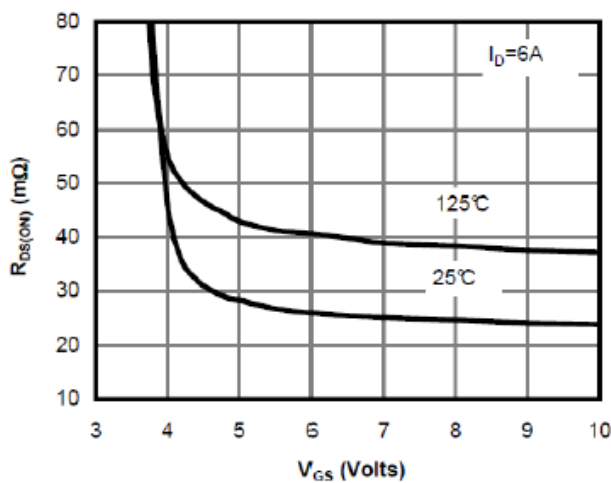


Figure 5: On-Resistance vs. Gate-Source Voltage

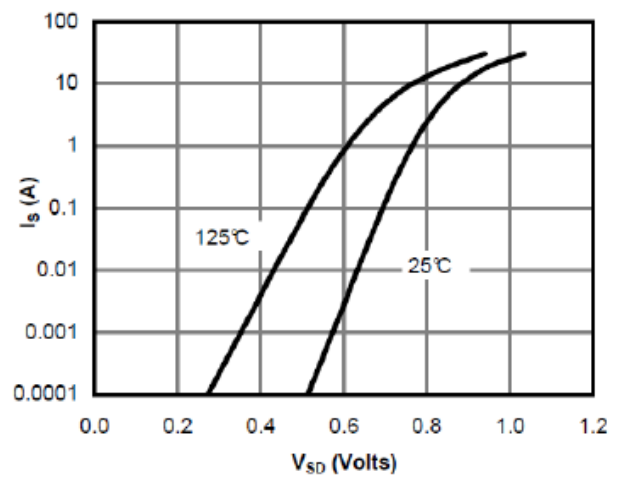


Figure 6: Body-Diode Characteristics

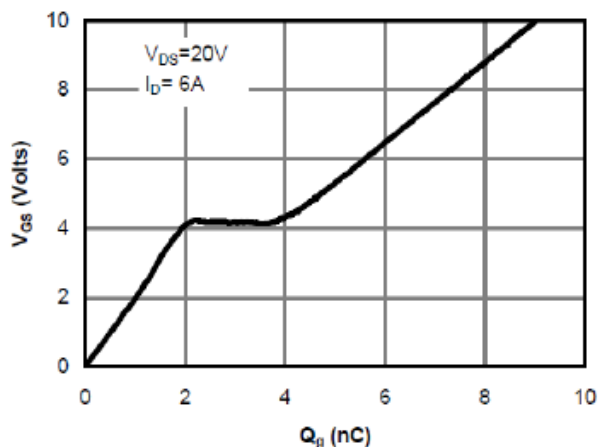


Figure 7: Gate-Charge Characteristics

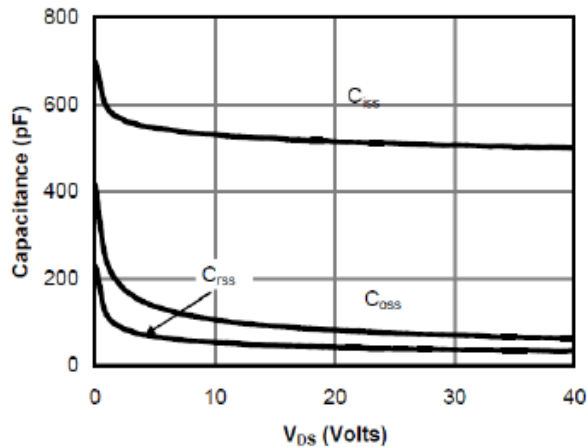


Figure 8: Capacitance Characteristics

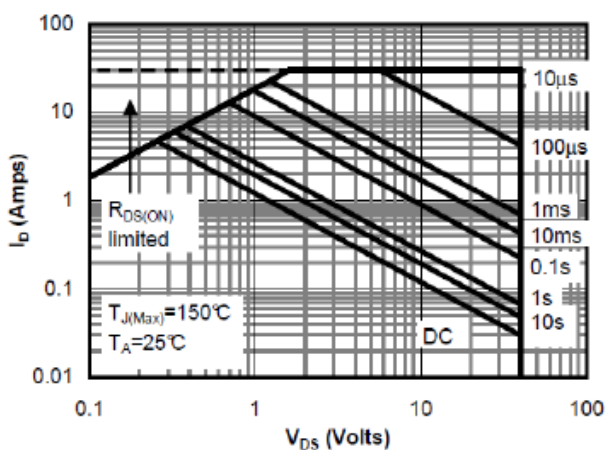


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

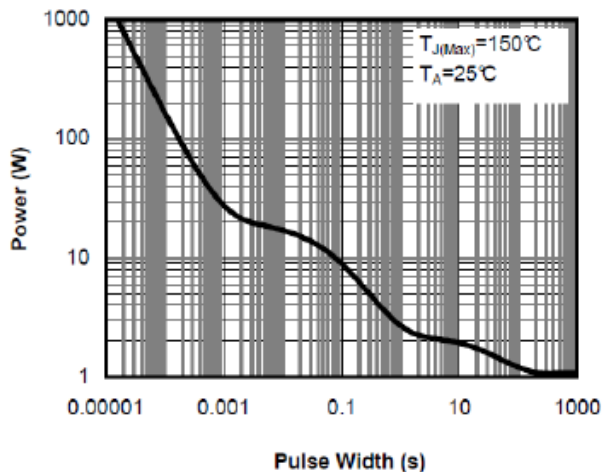


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

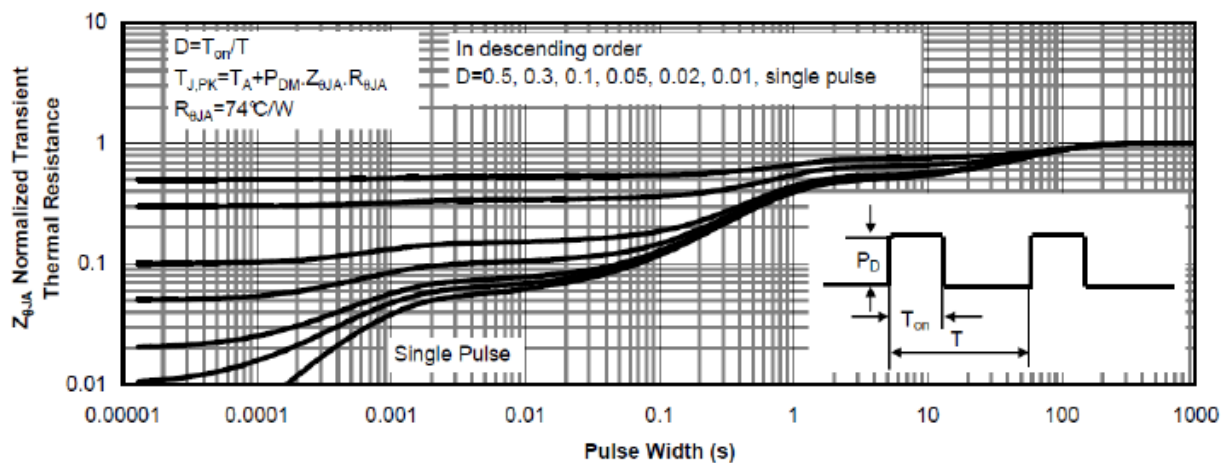


Figure 11: Normalized Maximum Transient Thermal Impedance



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