Dual P-Channel Enhancement Mode Field Effect Transistor

Features

V_{DS} (V) = -20V

I_D (V_{GS} = -4.5V)= -3A

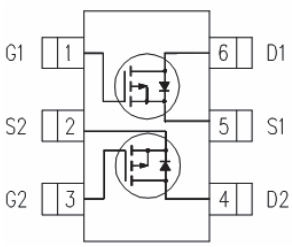
$R_{DS(ON)}$<85mΩ @ V_{GS}= -4.5V

$R_{DS(ON)}$<115mΩ @ V_{GS}= -2.5V

$R_{DS(ON)}$<150mΩ @ V_{GS}= -1.8V

SOT23-6L Package

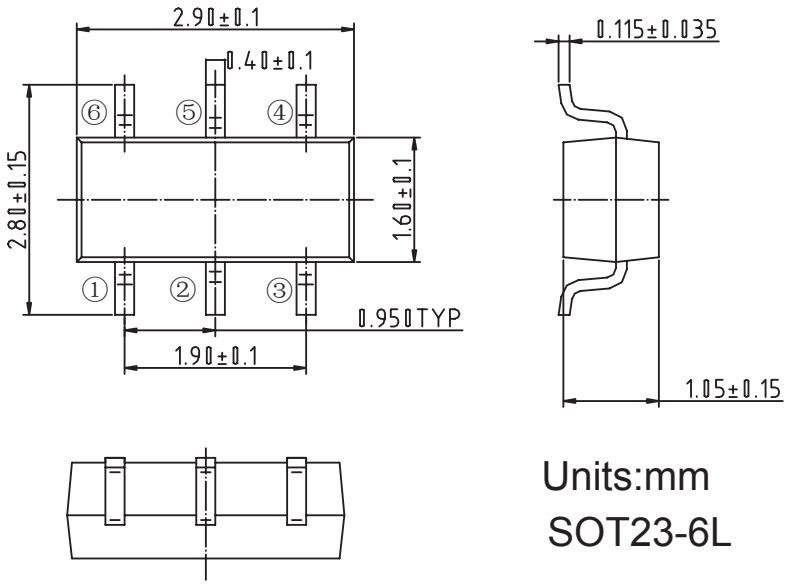
Pin Configurations



General Description

The HX1591 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. Standard Product HX1591 is Pb-free. HX1591L is a Green Product ordering option. HX1591 and HX1591L are electrically identical.

Package Information



Absolute Maximum Ratings @T_A=25℃ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±8	V
Drain Current (Continuous)	T_A=25°C	I_D	-3	A
	T_A=70°C		-2.4	
Drain Current (Pulse)[C]		I_{DM}	-13	A

Power Dissipation [B]	T_A=25°C	P_D	1.15	W
	T_A=70°C		0.73	W
Operating Temperature/ Storage Temperature		T_J/T_{STG}	-55~150	℃

- **Electrical Characteristics** @T_A=25℃ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ON/OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D= -250μA	-20	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20 V , V_{GS} = 0V	--	--	-1	μA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS} , I_{DS}= -250μA	-0.5	-0.6	-1	V
Gate Leakage Current	I_{GSS}	V_{GS}= ±8V , V_{DS}=0V	--	--	±100	nA
Drain-Source On-state Resistance	$R_{DS(on)}$	V_{GS} = -4.5V , I_D= -2.8A	--	80	85	mΩ
		V_{GS} = -2.5V , I_D= -2A	--	95	115	mΩ
		V_{GS} = -1.8V , I_D= -2A	--	119	150	mΩ
Forward Transconductance	g_{FS}	V_{DS}= -5V , I_D= -2.5A	--	13	--	S
Diode Forward Voltage	V_{SD}	I_{SD}= -1.6A , V_{GS}= 0V	--	-0.81	-1.0	V
Maximum Body-Diode Continuous Current	I_S		--	--	-1.6	A
Switching CHARACTERISTICS						
Total Gate Charge	Q_g	V_{DS} = -6V, I_D = -2.8A V_{GS} = -4.5V	--	6.6	8.6	nC
Gate-Source Charge	Q_{gs}		--	0.3	0.4	nC
Gate-Drain Charge	Q_{gd}		--	1.3	1.7	nC
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -6V, RL=6Ω I_D = -1A, V_{GEN} = -4.5V R_G = 6Ω	--	9.7	19.4	ns
Turn-on Rise Time	tr		--	3.6	7.1	ns
Turn-off Delay Time	$t_{d(off)}$		--	33.3	66.6	ns
Turn-off Fall Time	tf		--	4.5	9	ns
Dynamic CHARACTERISTICS						
Input Capacitance	Ciss	V_{GS}=0V,V_{DS}= -6V,f= 1.0MHz	--	589	--	pF
Output Capacitance	Coss		--	91.2	--	pF
Reverse Transfer Capacitance	Crss		--	67.2	--	pF

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using≤10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

- **Typical Performance Characteristics**

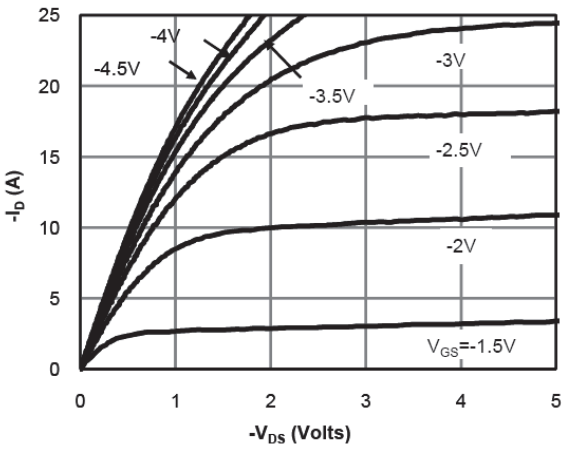


Figure 1: On-Region Characteristics

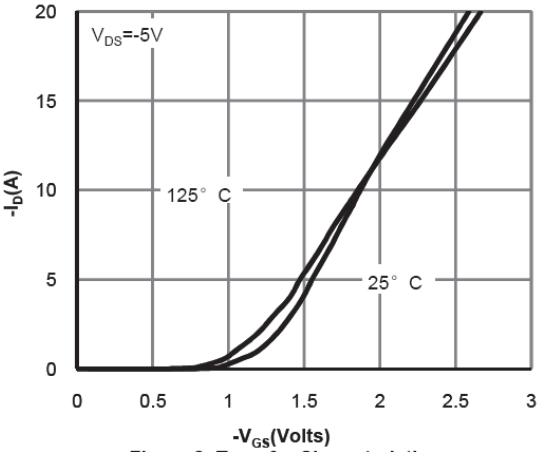


Figure 2: Transfer Characteristics

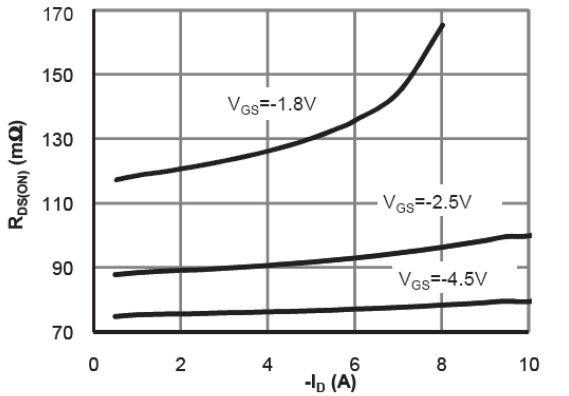


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

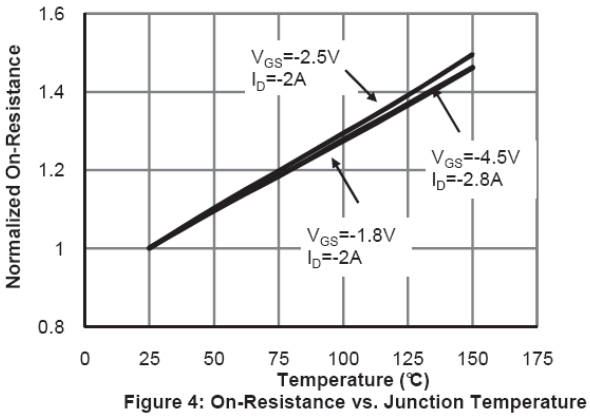


Figure 4: On-Resistance vs. Junction Temperature

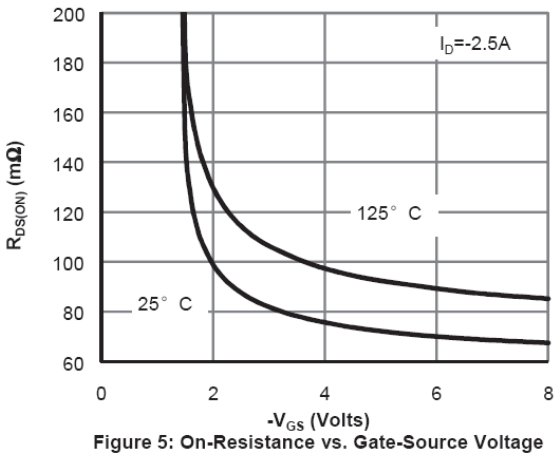


Figure 5: On-Resistance vs. Gate-Source Voltage

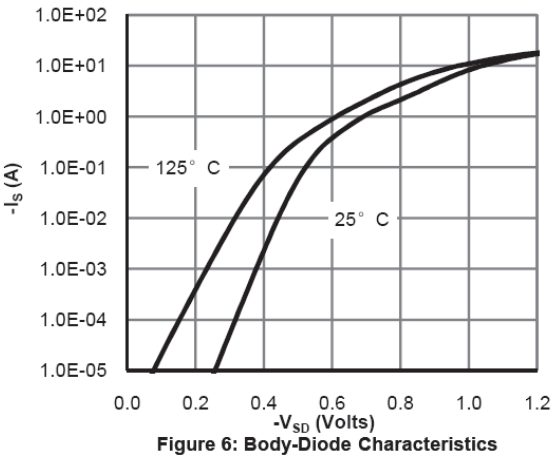


Figure 6: Body-Diode Characteristics

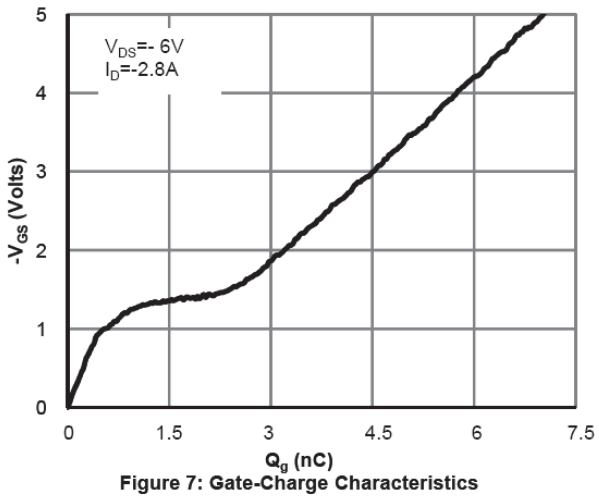


Figure 7: Gate-Charge Characteristics

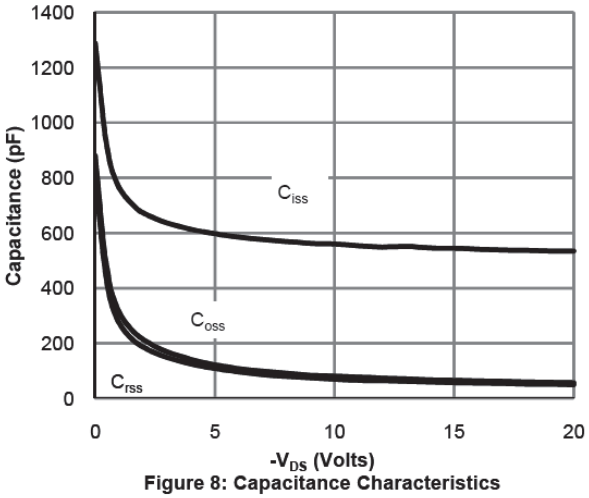


Figure 8: Capacitance Characteristics

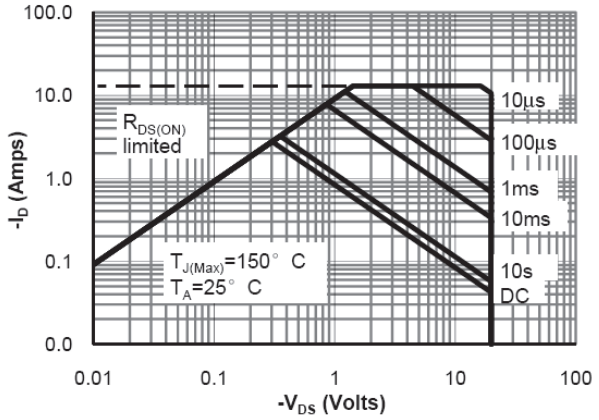


Figure 9: Maximum Forward Biased Safe Operating Area

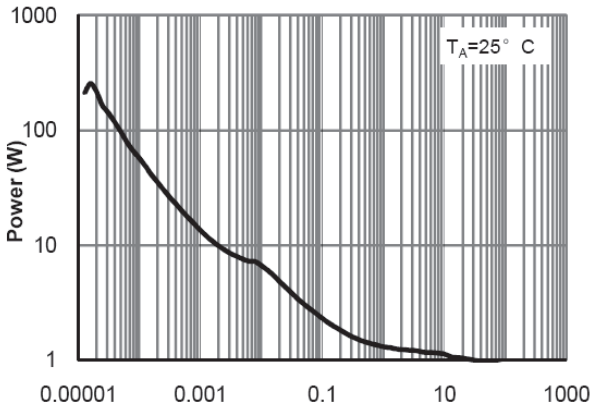


Figure 10: Single Pulse Power Rating Junction-to-Ambient

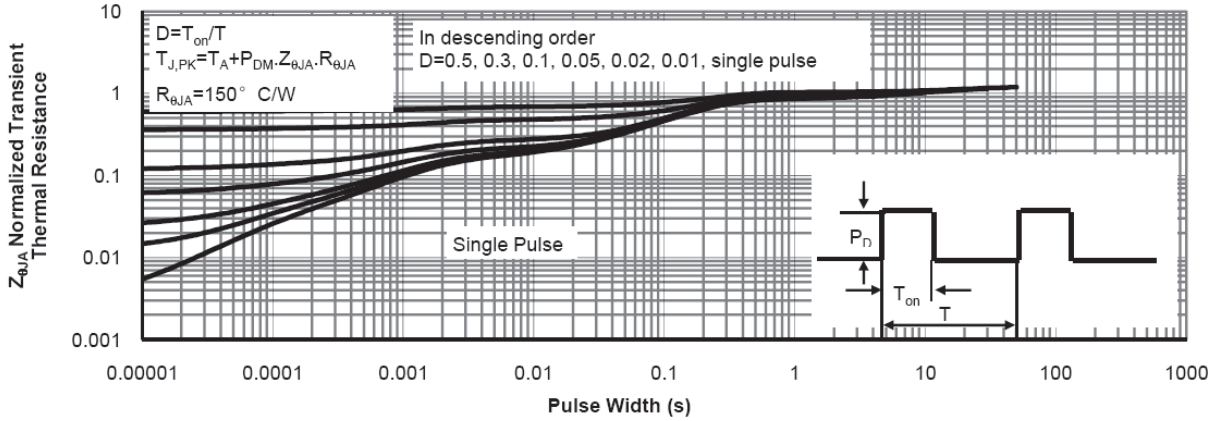


Figure 11: Normalized Maximum Transient Thermal Impedance

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